

**REMARKS**

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-12 are pending. Claims 1-12 are rejected. No claims have been objected to.

Claims 2 and 11-12 have been amended. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

**Claim Rejections – 35 U.S.C. § 103**

The Examiner has rejected claims 1-12 under 35 U.S.C. §103(a) as being unpatentable over Gephardt et al. (European Patent Application 0676686 A2), hereinafter “Gephardt” in view of Klein (US Patent No. 6,029,223), hereinafter “Klein”. For the reasons set forth below Applicants assert that the cited references fail to teach, suggest, or render obvious Applicants’ invention as claimed in claims 1-12.

Gephardt discloses “[an] integrated processor... include[ing] a power management message unit coupled to... [an] interrupt controller... for monitoring the internal interrupt and bus request signals of the integrated processor.” (Gephardt abstract, lines 5-9) Gephardt’s interrupt controller (Gephardt, Figure 2, Item 224) is located specifically within the integrated processor (Gephardt, Figure 2, Item 202). In the response, Examiner specifically refers to “the system 200 in figure 2 as a system logic device thus, the interrupt controller is located within the system 200.”

Klein discloses “[a] computer system having an advanced programmable interrupt controller (APIC)... in which an I/O APIC module is included in core logic circuitry coupled between a processor bus and a system bus.” (Klein abstract, lines 1-4) Klein has an I/O APIC module integrated within the microprocessor and another I/O APIC module integrated within the system controller.

With respect to independent claim 1 in the presently claimed invention, Applicants teach and claim “A method, comprising asserting an edge-triggered interrupt signal from an input/output interrupt controller located within a system logic device to a local interrupt controller located within a processor, and delivering an interrupt pending signal from the processor to a power management unit located within the system logic device.” (Applicants’ claim 1) Applicants’ invention as claimed in claim 1 specifies a system logic device (as one component of a system) that is entirely dissimilar to Gephardt’s system referred to in Examiner’s response.

The system logic device in Applicants’ invention is further described in the specification and Figure 1 of Applicants’ patent application. Referring to Applicants’ Figure 1, Applicants explicitly show a system (Applicants’ Figure 1, Item 100), which is comprised of a processor (Applicants’ Figure 1, Item 110) coupled to a system logic device (Applicants’ Figure 1, Item 120). Applicants’ system logic device is clearly shown as one device in the system, and the system is comprised of more than one device. Applicants’ input/output interrupt controller (Applicants’ Figure 1, Item 122) is located specifically within the system logic device. Examiner concludes in his response that Gephardt’s system (Gephardt’s Figure 2, Item 200) is equivalent and can be referred to as Applicants’ system logic device, thus the interrupt controller located within the

Gephardt's system is equivalent to the input/output controller located within Applicants' system logic device. Applicants respectfully disagree.

Applicants' system logic device by itself is not equivalent to Gephardt's entire system and cannot be logically compared as such because Applicants' system logic device is only one component of a system. Examiner's suggestion that Applicants' system logic device is equivalent to Gephardt's system suggests that all of the components of Gephardt's system, including the integrated processor (Gephardt's Figure 2, Item 202), the external bus (Gephardt's Figure 2, Item 206), and the peripheral device (Gephardt's Figure 2, Item 204) may be incorporated within Applicants' system logic device. This is entirely incorrect. Instead, the system logic device in Applicants' presently claimed invention is just one particular component of Applicants' larger system. Thus, in no way can Gephardt's system be viewed as analogous to Applicants' system logic device as Examiner suggests. Accordingly, Gephardt's placement of the interrupt controller (Gephardt Figure 2, Item 224) within the Gephardt's system is not equivalent to Applicants' placement of the input/output interrupt controller within Applicants' system logic device. Thus, Gephardt does not teach, suggest, or render obvious Applicants' invention as claimed in claim 1.

Even though Klein does describe an I/O APIC incorporated in core circuitry logic and an I/O APIC incorporated in a system controller, neither Gephardt nor Klein, taken alone or in combination, teaches "[a] method comprising asserting an edge-triggered interrupt signal from an input/output interrupt controller located within a system logic device to a local interrupt controller located within a processor, and delivering an interrupt pending signal from the processor to a power management unit located within

the system logic device.” Again, contrary to Examiner’s claim that “the system 200 in figure 2 as a system logic device thus, the interrupt controller is located within the system 200,” Applicants’ system logic device by itself is not equivalent, nor even similar, to Gephardt’s entire system and therefore Gephardt’s placement of the interrupt controller within the Gephardt’s system is not equivalent to Applicants’ placement of the input/output interrupt controller within Applicants’ system logic device. Thus, Applicants respectfully submit that Gephardt and Klein, taken alone or in combination, do not render independent claim 1 as obvious.

Claims 2-4 are dependent upon independent claim 1. Thus, for at least the same reasons advanced above with respect to independent claim 1, Applicants respectfully submit that Gephardt and Klein, taken alone or in combination, do not render these dependent claims obvious.

In regard to independent claims 5 and 9, the cited reference fails to teach or render obvious Applicants’ invention for the same reason as independent claim 1. Again, Gephardt and Klein, taken alone or in combination, do not teach “[a] method comprising asserting an edge-triggered interrupt signal from an input/output interrupt controller located within a system logic device to a local interrupt controller located within a processor.” Thus, Gephardt and Klein, taken alone or in combination, do not teach all the elements in each of the claims. Therefore, since all the elements are not met by Gephardt and Klein, Applicants respectfully submit that Gephardt and Klein, taken alone or in combination, do not render independent claims 5 and 9 obvious.

Claims 6-8 are dependent upon independent claim 5. Thus, for at least the same reasons advanced above with respect to independent claim 5, Applicants respectfully submit that Gephardt and Klein, taken alone or in combination, do not render these dependent claims obvious.

Claims 10-12 are dependent upon independent claim 9. Thus, for at least the same reasons advanced above with respect to independent claim 9, Applicants respectfully submit that Gephardt and Klein, taken alone or in combination, do not render these dependent claims obvious.

Thus, Gephardt and Klein, taken alone or in combination, do not teach, suggest, or render obvious Applicants' invention as claimed in pending claims 1-12. Applicants respectfully request withdrawal of the 35 U.S.C. 103(a) rejection of claims 1-12.



If there are any additional charges, please charge Deposit Account No 02-2666.

If a telephone conference would facilitate the prosecution of this application, the

Examiner is invited to contact Michael J. Mallie at (408) 720-8300.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: 8/20/04 [Signature]

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